WHAT IS CLAIMED IS:

1. A precoding-multiplexing circuit, comprising:

a precoding circuit for carrying out a precoding with respect to n sets of parallel input binary data signals having a bit rate equal to R/n, to obtain n sets of parallel precoded signals; and

a time division multiplexer for time division multiplexing the parallel precoded signals obtained by the precoding circuit, in units of one bit, and outputting a time division multiplexed output signal having a bit rate equal to R.

2. The precoding-multiplexing circuit of claim 1, wherein the precoding circuit carries out the precoding such that the time division multiplexed output signal outputted by the time division multiplexer is equivalent to a signal that can be obtained by precoding a binary data signal having a bit rate equal to R that is time division multiplexed in units of one bit in advance.

3. The precoding-multiplexing circuit of claim 2, wherein the precoding circuit further comprises:

a first EXOR circuit for calculating a first exclusive OR value of all of the n set of the parallel input binary data signals;

a differential encoder for obtaining an encoded signal by maintaining an output logical value for the first input logical value while inverting an output logical value for the second input logical value in the first exclusive OR value calculated by the first EXOR circuit, and delaying for one time-slot time with respect to the parallel input binary data signals; and

(n-1) sets of second EXOR circuits provided in correspondence to all but one of the n sets of the parallel

input binary data signals, a first one of the second EXOR circuits calculating a second exclusive OR value of a corresponding one of the parallel input binary data signals and the encoded signal obtained by the differential encoder, and each of second to (n-1)-th ones of the second EXOR circuits calculating a second exclusive OR value of a corresponding one of the parallel input binary data signals and an output of an immediately previous second EXOR circuit;

wherein the encoded signal obtained by the differential encoder and the second exclusive OR values calculated by the second EXOR circuits are outputted as the parallel precoded signals.

4. The precoding-multiplexing circuit of claim 3, wherein the first EXOR circuit is formed by a combination of (n-1) sets of EXOR circuits.

5. The precoding-multiplexing circuit of claim 3, wherein the differential encoder further comprises:

an EXOR circuit having one input connected to an input of the differential encoder; and

a delay for delaying an output of the EXOR circuit for one time-slot time;

wherein an output of the delay is fed back to another input of the EXOR circuit while also outputted as an output of the differential encoder.

6. The precoding-multiplexing circuit of claim 3, wherein the differential encoder further comprises:

an EXOR circuit having one input connected to an input of the differential encoder; and

a D-type flip-flop connected to an output of the EXOR circuit and formed by a master latch and a slave latch, an output of the master latch being fed back to another input

of the EXOR circuit while also entered into the slave latch, and an output of the slave latch being outputted as an output of the differential encoder.

7. The precoding-multiplexing circuit of claim 3, wherein the differential encoder further comprises:

(n-1) sets of first delay units connected in series, for sequentially delaying an input of the differential encoder, for one time-slot time at each first delay unit;

a third EXOR circuit for calculating an exclusive OR value of all of the input of the differential encoder and (n-1) sets of outputs of the first delay units;

a fourth EXOR circuit having one input connected to an output of the third EXOR circuit, an output of the fourth EXOR circuit being outputted as an output of the differential encoder; and

a second delay unit for delaying an output of the fourth EXOR circuit for n time-slot time, an output of the second delay unit being fed back to another input of the fourth EXOR circuit.

8. The precoding-multiplexing circuit of claim 7, wherein the third EXOR circuit is formed by a combination of (n-1) sets of EXOR circuits.

9. The precoding-multiplexing circuit of claim 2, wherein n = 2 such that the parallel input binary data signals include a preceding signal which is to be time division multiplexed earlier and a subsequent signal which is to be time division multiplexed later, and the precoding circuit further comprises:

a first delay unit for delaying the subsequent signal for one half time-slot time;

a first EXOR circuit having one input to which the preceding signal is entered;

a second EXOR circuit having one input to which the subsequent signal as delayed by the first delay unit is entered;

a second delay unit for delaying an output of the first EXOR circuit for one half time-slot time;

a third delay unit for delaying an output of the second EXOR circuit for one half time-slot time; and

a reset unit for resetting initial states of outputs of the first EXOR circuit and the second EXOR circuit;

wherein an output of the second delay unit is fed back to another input of the first EXOR circuit while an output of the third delay unit is fed back to another input of the second EXOR circuit, and outputs of the second delay unit and the third delay unit are outputted as the parallel precoded signals.

10. The precoding-multiplexing circuit of claim 9, wherein the time division multiplexer obtains the time division multiplexed output signal by alternately selecting the output of the second delay unit and the output of the third delay unit as constituents of the time division multiplexed output signal.

11. The precoding-multiplexing circuit of claim 1, further comprising:

a time division demultiplexer for time division demultiplexing binary data signals having a bit rate equal to R, into the n sets of the parallel input binary data signals having a bit rate equal to R/n which are entered into the precoding circuit.

12. A precoding circuit, comprising:

an input receiving n sets of paralle input binary data signals having a bit rate equal to R/n;

a precoder for carrying out a precoding with respect

to the parallel input binary data signals, to obtain n sets of parallel precoded signals, such that time division multiplexed signals having a bit rate equal to R that can be obtained by time division multiplexing the parallel precoded signals will be equivalent to signals that can be obtained by precoding n sets of binary data signals that are time division multiplexed in units of one bit in advance; and

an output outputting the parallel precoded signals obtained by the precoder.

13. The precoding circuit of claim 12, wherein the precoder further comprises:

a first EXOR circuit for calculating a first exclusive OR value of all of the n set of the parallel input binary data signals;

a differential encoder for obtaining an encoded signal by maintaining an output logical value for the first input logical value while inverting an output logical value for the second input logical value in the first exclusive OR value calculated by the first EXOR circuit, and delaying for one time-slot time with respect to the parallel input binary data signals; and

(n-1) sets of second EXOR circuits provided in correspondence to all but one of the n sets of the parallel input binary data signals, a first one of the second EXOR circuits calculating a second exclusive OR value of a corresponding one of the parallel input binary data signals and the encoded signal obtained by the differential encoder, and each of second to (n-1)-th ones of the second EXOR circuits calculating a second exclusive OR value of a corresponding one of the parallel input binary data signals and an output of an immediately previous second EXOR circuit;

wherein the encoded signal obtained by the

differential encoder and the second exclusive OR values calculated by the second EXOR circuits are outputted as the parallel precoded signals.

14. The precoding-multiplexing circuit of claim 13, wherein the third EXOR circuit is formed by a combination of (n-1) sets of EXOR circuits.

15. The precoding circuit of claim 13, wherein the differential encoder further comprises:

an EXOR circuit having one input connected to an input of the differential encoder; and

a delay for delaying an output of the EXOR circuit for one time-slot time;

wherein an output of the delay is fed back to another input of the EXOR circuit while also outputted as an output of the differential encoder.

16. The precoding circuit of claim 13, wherein the differential encoder further comprises:

an EXOR circuit having one input connected to an input of the differential encoder; and

a D-type flip-flop connected to an output of the EXOR circuit and formed by a master latch and a slave latch, an output of the master latch being fed back to another input of the EXOR circuit while also entered into the slave latch, and an output of the slave latch being outputted as an output of the differential encoder.

17. The precoding circuit of claim 13, wherein the differential encoder further comprises:

(n-1) sets of first delay units connected in series, for sequentially delaying an input of the differential encoder, for one time-slot time at each first delay unit;

a third EXOR circuit for calculating an exclusive OR

value of all of the input of the differential encoder and (n-1) sets of outputs of the first delay units;

a fourth EXOR circuit having one input connected to an output of the third EXOR circuit, an output of the fourth EXOR circuit being outputted as an output of the differential encoder; and

a second delay unit for delaying an output of the fourth EXOR circuit for n time-slot time, an output of the second delay unit being fed back to another input of the fourth EXOR circuit.

18. The precoding circuit of claim 17, wherein the third EXOR circuit is formed by a combination of (n-1) sets of EXOR circuits.

19. The precoding circuit of claim 12, wherein n = 2 such that the parallel input binary data signals include a preceding signal which is to be time division multiplexed earlier and a subsequent signal which is to be time division multiplexed later, and the precoding circuit further comprises:

a first delay unit for delaying the subsequent signal for one half time-slot time;

a first EXOR circuit having one input to which the preceding signal is entered;

a second EXOR circuit having one input to which the subsequent signal as delayed by the first delay unit is entered;

a second delay unit for delaying an output of the first EXOR circuit for one half time-slot time;

a third delay unit for delaying an output of the second EXOR circuit for one half time-slot time; and

a reset unit for resetting initial states of outputs of the first EXOR circuit and the second EXOR circuit;

wherein an output of the second delay unit is fed back

to another input of the first EXOR circuit while an output of the third delay unit is fed back to another input of the second EXOR circuit, and outputs of the second delay unit and the third delay unit are outputted as the parallel precoded signals.

20. The precoding circuit of claim 12, further comprising:

a time division demultiplexer for time division demultiplexing binary data signals having a bit rate equal to R, into the n sets of the parallel input binary data signals having a bit rate equal to R/n which are entered into the input of the precoding circuit.

21. A differential encoder for carrying out a precoding with respect to input binary data signals, to obtain encoded signals in which an output logical value is maintained for a first input logical value while an output logical value is inverted for a second input logical value, comprising:

an EXOR circuit having one input to which the input binary data signals are entered; and

a D-type flip-flop connected to an output of the EXOR circuit and formed by a master latch and a slave latch, an output of the master latch being fed back to another input of the EXOR circuit while also entered into the slave latch, and an output of the slave latch being outputted as an output of the differential encoder.

22. A differential encoder for carrying out a precoding with respect to input binary data signals, to obtain encoded signals in which an output logical value is maintained for a first input logical value while an output logical value is inverted for a second input logical value, comprising:

(n-1) sets of first delay units connected in series,

for sequentially delaying an input of the differential encoder, for one time-slot time at each first delay unit;

a first EXOR circuit for calculating an exclusive OR value of all of the input of the differential encoder and (n-1) sets of outputs of the first delay units;

a second EXOR circuit having one input connected to an output of the first EXOR circuit, an output of the second EXOR circuit being outputted as an output of the differential encoder; and

a second delay unit for delaying an output of the second EXOR circuit for n time-slot time, an output of the second delay unit being fed back to another input of the second EXOR circuit.

23. The differential encoder of claim 22, wherein the first EXOR circuit is formed by a combination of (n-1) sets of EXOR circuits.